Cache Specification

**Step I. ALL DIRECT-MAPPED**

L1 Cache:

1. Total Words: 32 words

2. 8 blocks and 4 words each

3. Policy: Write-back

L2 Cache:

1. Total Words: 256 words

2. 64 blocks and 4 words each

3. Policy: Write-back

L2 Architectures

|  |  |  |
| --- | --- | --- |
| Port | I/O Type | Spec |
| clock | input |  |
| L2 reset | input |  |
| L2 read / write | input |  |
| L1 address | input | 28 bits |
| L1 write data | input | 32 bits |
| L2 ready | output |  |
| L1 read data | output | 128 bits (4 words) |
|  |  |  |
| memory read | output |  |
| memory write | output |  |
| memory address | output | 20 bits, minus 8 bits |
| memory write data | output | 128 bits |
| memory read data | input | 128 bits |
| memory ready | input |  |